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10/716,008	11/18/2003	Lakshman Ramakrishnan	15030US02	4199

  

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EXAMINER	
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ART UNIT	PAPER NUMBER
2621	

  

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10/03/2007	PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/716,008	RAMAKRISHNAN ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Behrooz Senfi	2621	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 18 November 2003.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-8 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-8 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 09 August 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)          | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

**DETAILED ACTION**

***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1 and 5 are rejected under 35 U.S.C. 102(e) as being anticipated by Yoshioka et al. (US 7,079,583).

Regarding claim 1, Yoshioka '583 discloses, a method for storing macro-blocks in a memory (i.e., fig. 3, memory 3 is used for storing macro-blocks); the method comprising;

decoding a macro-block (i.e., fig. 3, decoder 1002 including routine processing 1004 used for decoding a macro-block, see col. 11, lines 39 – 44 and col. 16, lines 12 – 13); and

executing an instruction, wherein the instruction causes writing the macro-block to the memory (i.e., fig. 3, illustrates decoder unit 1002 including, routine processing unit 1004 execute the received instruction from processing unit 1003 to perform decode processing on macro-block and stores/writes the decoded block/macro-block to the memory unit 3, see col. 11, lines 39 – 50).

Regarding claim 5, Yoshioka '583 discloses, a circuit for storing macro-blocks (i.e., external memory 3 in the circuits as shown in fig. 3 is used for storing macro-blocks), circuit comprising;

a decoder for decoding macro-blocks (i.e., fig. 3, decoder 1002 used for decoding macro-blocks, see col. 11, lines 39 – 44); and

a computer readable medium storing an executable instruction (i.e., figs. 3 - 4, it is cleared that the software/instruction is necessitated by the processing units as shown in figs. 3 - 4 in order to carry on the process; such as, decoding macro-blocks, see col. 3, lines 51 – 67 and col. 11, lines 39 - 50), wherein the instruction causes, writing the macro-block to the memory (i.e., as shown in fig. 3, the decoded block/macro-block is written/stored to the memory unit 3, see col. 11, lines 39 – 50).

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 2 – 4 and 6 - 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshioka et al. (US 7,079,583) in view of Uchida (US 5,461,486).

Regarding claim 2, Yoshioka '583 teaches, Yoshioka '583 teaches, writing the macro-block to the memory, as discussed with respect to claim 1 above (i.e., as shown in fig. 3, the decoded block/macro-block is written/stored to the memory unit 3, see col. 11, lines 39 – 50 and col. 14, lines 30 - 32), further comprises;

Although, Yoshioka '583 show writing macro-block composed of luminance matrix blocks (Y) and chrominance matrix blocks (Cb) and (Cr) to the memory, Yoshioka '583 is silent in regards to explicit of, "writing a luminance matrix to a first portion of the memory; writing a first chrominance matrix to second portion of the memory; writing a second chrominance matrix to a third portion of the memory; and the first portion, second portion, and third portion being contiguous".

Uchida '486 teaches the above-mentioned claimed limitations are well known in the art. In particular, Uchida '486 teaches, writing a luminance matrix to a first portion of the memory (i.e., as shown in fig. 11, the DCT blocks of luminance Y matrix are stored in the respective memory areas assigned to, e.g., first portion of memory, see col. 7, lines 40 – 41 and lines 55 – 60); writing a first chrominance matrix to second portion of the memory (i.e., as shown in fig. 11, the DCT blocks of the color difference R-Y, e.g., first chrominance matrix (Cr) stored in the respective memory area assigned thereto, e.g., second portion of memory, see col. 7, lines 40 – 41 and lines 55 – 60); writing a second chrominance matrix to a third portion of the memory (i.e., as shown in fig. 11, the DCT blocks of second chrominance matrix B-Y (Cb) written/stored in the respective memory area assigned thereto, e.g., third portion of the memory, see col. 7, lines 40 – 41 and lines 55 – 60); and the first portion, second portion, and third portion being contiguous (i.e., as shown in fig. 11, the first portion (Y), second portion (R-Y) and third portion (B-Y) of the memory are arranged in continuous/contiguous form).

In view of the above, having the digital signal processing of Yoshioka showing writing decoded macro-block composed of luminance blocks (Y) and chrominance

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blocks (Cb) and (Cr) to the memory, and given the well-established teaching of Uchida where the luminance matrix is written in a first portion of the memory; and first chrominance matrix to second portion of the memory and a second chrominance matrix to a third portion of the memory, where the first portion, second portion, and third portion being contiguous, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the digital signal processing of Yoshioka as taught by Uchida, since Uchida suggest in col. 2, lines 57 – 58 that such a modification would improved image quality in the high speed reproduction of the recorded digital video signal.

Regarding claim 3, Yoshioka '583 teaches, a method for storing macro-blocks In a memory (i.e., fig. 3, memory 3 is used for storing macro-blocks), the method comprising;

decoding macro-blocks (i.e., fig. 3, decoder 1002 including routine processing 1004 used for decoding a macro-blocks, see col. 11, lines 40 – 43 and col. 16, lines 12 – 13); and

executing an instruction, wherein the instruction causes writing the macro-blocks to the memory (i.e., fig. 3, describes routine processing unit 1004 execute the received instruction from processing unit 1003 to perform decode processing on macro-blocks and stores/writes the decoded macro-block to the memory unit 3, see col. 11, lines 39 – 50).

Although, Yoshioka '583 teaches decoding macro-blocks and writing/storing macro-blocks to the memory, Yoshioka '583 is silent in regards to explicit of "five macro-blocks".

Uchida '486 teaches the above-mentioned claimed limitations are well known in the art. In particular, Uchida '486 teaches that, compression operation is applied to every five macro-blocks and writing five macro-blocks to the memory areas (i.e., col. 7, lines 40 – 41, col. 15, lines 20 – 21).

In view of the above, having the digital signal processing of Yoshioka showing compression operation is applied to macro-blocks and writing/storing decoded macro-blocks to the memory, and given the well-established teaching of Uchida where the compression operation is applied to every five macro-blocks and writing five macro-blocks to the memory areas, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the digital signal processing of Yoshioka as taught by Uchida, since Uchida suggest in col. 2, lines 57 – 58 that such a modification would improved image quality in the high speed reproduction of the digital video signal.

Regarding claim 4, the combination of Yoshioka '583 and Uchida '486 teaches, writing the five macro-block to the memory, as discussed with respect to claim 3 above, further comprises; writing five luminance matrices to the first five portions of the memory (please see, col. 7, lines 40 – 41 of Uchida, indicating five macro-blocks is written in five memory areas, and further fig. 11 of Uchida, illustrates the order that a macro-block is written in the memory areas, luminance matrices Y is written to the first

portion of the memory as shown in fig. 11, see col. 7, lines 44 – 57 of Uchida, it is cleared that each one of the five macro-blocks would be written to the memory in the same order as shown in fig. 11 for each macro-block, e.g., five luminance matrices Y would be written to the first five portion of the memory);

writing five chrominance matrix to a second five portions of the memory (please see, col. 7, lines 40 – 41 of Uchida, indicating five macro-blocks is written in five memory areas, and further fig. 11 of Uchida, illustrates the order that a macro-block is written in the memory areas, chrominance matrix R-Y (Cr) is written to the second portion of the memory as shown in fig. 11, see col. 7, lines 44 – 57 of Uchida, it is cleared that each one of the five macro-blocks would be written to the memory in the same order as shown in fig. 11 for each macro-block, e.g., five chrominance matrix R-Y (Cr) would be written to a second five portions of the memory);

writing five chrominance matrix to a third five portions of the memory; (please see, col. 7, lines 40 – 41 of Uchida, indicating five macro-blocks is written in five memory areas, and further fig. 11 of Uchida, illustrates the order that a macro-block is written in the memory areas, chrominance matrix B-Y (Cb) is written to the third portion of the memory as shown in fig. 11, see col. 7, lines 44 – 57 of Uchida, it is cleared that each one of the five macro-blocks would be written to the memory in the same order as shown in fig. 11 for each macro-block, e.g., five chrominance matrix B-Y (Cb) would be written to a third five portions of the memory); and

the first five portions, second five portions, and third five portions being contiguous (i.e., fig. 11 of Uchida, illustrates the order that the luminance matrices Y



and Chrominance matrix (Cr) and (Cb) for each macro-block is written to the first, second and third portions of the memory in a continuous/contiguous manner, it is cleared that each one of the five macro-blocks would be written to the memory in the same order and in a continuous/contiguous manner as shown in fig. 11 of Uchida).

Regarding claim 6, Yoshioka '583 teaches, writing the macro-block to the memory, as discussed with respect to claim 1 above (i.e., as shown in fig. 3, the decoded block/macro-block is written/stored to the memory unit 3, see col. 11, lines 39 – 50 and col. 14, lines 30 - 32), further comprises;

Although, Yoshioka '583 show writing macro-block composed of luminance matrix blocks (Y) and chrominance matrix blocks (Cb) and (Cr) to the memory, Yoshioka '583 is silent in regards to explicit of, "writing a luminance matrix to a first portion of the memory; writing a first chrominance matrix to second portion of the memory; writing a second chrominance matrix to a third portion of the memory; and the first portion, second portion, and third portion being contiguous".

Uchida '486 teaches the above-mentioned claimed limitations are well known in the art. In particular, Uchida '486 teaches, writing a luminance matrix to a first portion of the memory (i.e., as shown in fig. 11, the DCT blocks of luminance Y matrix are stored in the respective memory areas assigned to, e.g., first portion of memory, see col. 7, lines 40 – 41 and lines 55 – 60); writing a first chrominance matrix to second portion of the memory (i.e., as shown in fig. 11, the DCT blocks of the color difference R-Y, e.g., first chrominance matrix (Cr) stored in the respective memory area assigned thereto, e.g., second portion of memory, see col. 7, lines 40 – 41 and lines 55 – 60); writing a

second chrominance matrix to a third portion of the memory (i.e., as shown in fig. 11, the DCT blocks of second chrominance matrix B-Y (Cb) written/stored in the respective memory area assigned thereto, e.g., third portion of the memory, see col. 7, lines 40 – 41 and lines 55 – 60); and the first portion, second portion, and third portion being contiguous (i.e., as shown in fig. 11, the first portion (Y), second portion (R-Y) and third portion (B-Y) of the memory are arranged in continuous/contiguous form).

In view of the above, having the digital signal processing of Yoshioka showing writing decoded macro-block composed of luminance blocks (Y) and chrominance blocks (Cb) and (Cr) to the memory, and given the well-established teaching of Uchida where the luminance matrix is written in a first portion of the memory; and first chrominance matrix to second portion of the memory and a second chrominance matrix to a third portion of the memory, where the first portion, second portion, and third portion being contiguous, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the digital signal processing of Yoshioka as taught by Uchida, since Uchida suggest in col. 2, lines 57 – 58 that such a modification would improved image quality in the high speed reproduction of the recorded digital video signal.

Regarding claim 7, Yoshioka '583 teaches, a circuit for storing macro-blocks (i.e., external memory 3 in the circuit as shown in fig. 3 is used for storing macro-blocks), circuit comprising;

a decoder for decoding macro-blocks (i.e., fig. 3, decoder 1002 is used for decoding macro-blocks, see col. 11, lines 40 – 43 and col. 16, lines 12 – 13); and

a computer readable medium storing an executable instruction (i.e., figs. 3 - 4, it is cleared that the software/instruction is necessitated by the processing units as shown in figs. 3 - 4 in order to carry on the process; such as, decoding macro-blocks, see col. 3, lines 51 - 67 and col. 11, lines 39 - 50), wherein the instruction causes, writing the macro-block to the memory (i.e., as shown in fig. 3, the decoded block/macro-block is written/stored to the memory unit 3, see col. 11, lines 39 - 50 of Yoshioka).

Although, Yoshioka '583 teaches decoding macro-blocks and writing/storing macro-blocks to the memory, Yoshioka '583 is silent in regards to explicit of "five macro-blocks".

Uchida '486 teaches the above-mentioned claimed limitations are well known in the art. In particular, Uchida '486 teaches that, compression operation is applied to every five macro-blocks and writing five macro-blocks to the memory areas (i.e., col. 7, lines 40 - 41, col. 15, lines 20 - 21).

In view of the above, having the digital signal processing of Yoshioka showing compression operation is applied to macro-blocks and writing/storing decoded macro-blocks to the memory, and given the well-established teaching of Uchida where the compression operation is applied to every five macro-blocks and writing five macro-blocks to the memory areas, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the digital signal processing of Yoshioka as taught by Uchida, since Uchida suggest in col. 2, lines 57 - 58 that such a modification would improved image quality in the high speed reproduction of the digital video signal.

Regarding claim 8, the combination of Yoshioka '583 and Uchida '486 teaches, writing the five macro-block to the memory, as discussed with respect to claim 3 above, further comprises; writing five luminance matrices to the first five portions of the memory (please see, col. 7, lines 40 – 41 of Uchida, indicating five macro- blocks is written in five memory areas, and further fig. 11 of Uchida, illustrates the order that a macro-block is written in the memory areas, luminance matrices Y is written to the first portion of the memory as shown in fig. 11, see col. 7, lines 44 – 57 of Uchida, it is cleared that each one of the five macro-blocks would be written to the memory in the same order as shown in fig. 11 for each macro-block, e.g., five luminance matrices Y would be written to the first five portion of the memory);

writing five chrominance matrix to a second five portions of the memory (please see, col. 7, lines 40 – 41 of Uchida, indicating five macro-blocks is written in five memory areas, and further fig. 11 of Uchida, illustrates the order that a macro-block is written in the memory areas, chrominance matrix R-Y (Cr) is written to the second portion of the memory as shown in fig. 11, see col. 7, lines 44 – 57 of Uchida, it is cleared that each one of the five macro-blocks would be written to the memory in the same order as shown in fig. 11 for each macro-block, e.g., five chrominance matrix R-Y (Cr) would be written to a second five portions of the memory);

writing five chrominance matrix to a third five portions of the memory; (please see, col. 7, lines 40 – 41 of Uchida, indicating five macro- blocks is written in five memory areas, and further fig. 11 of Uchida, illustrates the order that a macro-block is written in the memory areas, chrominance matrix B-Y (Cb) is written to the third portion of the

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memory as shown in fig. 11, see col. 7, lines 44 – 57 of Uchida, it is cleared that each one of the five macro-blocks would be written to the memory in the same order as shown in fig. 11 for each macro-block, e.g., five chrominance matrix B-Y (Cb) would be written to a third five portions of the memory); and

the first five portions, second five portions, and third five portions being contiguous (i.e., fig. 11 of Uchida, illustrates the order that the luminance matrices Y and Chrominance matrix (Cr) and (Cb) for each macro-block is written to the first, second and third portions of the memory in a continuous/contiguous manner, it is cleared that each one of the five macro-blocks would be written to the memory in the same order and in a continuous/contiguous manner as shown in fig. 11 of Uchida).

#### **Contact**

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Behrooz Senfi whose telephone number is 571-272-7339. The examiner can normally be reached on M-F 7:00-3:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mehrdad Dastouri can be reached on 571-272-7418. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Behrooz Senfi  
Examiner  
Art Unit 2621

